

APPLICATION FOR UNITED STATES LETTERS PATENT

by

MICHAEL BERNHARD SOMMER

for an

**INTEGRATED SEMICONDUCTOR MEMORY CIRCUIT AND METHOD OF
MANUFACTURING THE SAME**

SHAW PITTMAN LLP
1650 Tysons Boulevard
McLean, VA 22102-4859
(703) 770-7900
Attorney Docket No.:INF-126

INTEGRATED SEMICONDUCTOR MEMORY CIRCUIT AND METHOD OF MANUFACTURING THE SAME

BACKGROUND

FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated semiconductor circuits.

BACKGROUND INFORMATION

[0002] The implantation of n- and p-conducting wells in a semiconductor substrate gives rise to parameter fluctuations of the structures of the active components formed in the wells, such as transistors, for example, which stem from so-called "well scattering". Said well scattering occurs since, on account of the channeling effect, the ion beam, which brings about the implantation, is radiated in at a certain angle, namely not perpendicularly to the wafer surface, so that a bombardment angle parallel to the crystal planes is avoided. However, the consequence of said angle is that the ion beam is scattered at an edge formed by a step.

[0003] The effect of this scattering phenomenon is illustrated with reference to the accompanying Figure 1. Figure 1 diagrammatically shows a section at the surface of a semiconductor wafer in which an implantation is carried out by means of an ion beam B incident at an irradiation angle α . Said implantation is performed into a well 11, which is an n-doped well, for example. An adjacent region, for example a p-doped well 12, is covered by a photoresist layer 3, the left-hand edge of which defines a boundary G—depicted in dash-dotted fashion—between well region 11 and the adjacent well region 12.

[0004] Due to the required irradiation angle α , the ion beam B is scattered at the sidewall of the photoresist 3. However, the consequence of the scattering of the ion

beam B during the well implantation is that an additional, undesired and uncontrollable doping takes place at the substrate surface, as indicated by the lower pair of arrows originating at the left edge of photoresist 3 and terminating at a region 2. If this undesirable scattering of ion beam B at the sidewall of photoresist 3 contaminates region 2 of an active component, such as an FET, the affected transistor (and other components affected by this undesirable implantation contamination) may behave completely differently than the manner envisaged by the design and revealed by simulation. This leads to functional problems for the semiconductor circuit.

[0005] The problem outlined above has previously been solved by maintaining sufficient distance between the boundary G and active regions in the implanted well, such as region 2. That is to say, the active components have been positioned far enough away from the scattering beam. However, problems occur to an increased extent as feature sizes become increasingly smaller, as revealed in reduced fabrication yield and reduced device quality. In order to provide a remedy, so-called “quad implants” have been used specifically in the DRAM fabrication process. Thus, each individual memory bank has been individually implanted with a respectively alternating irradiation direction of the ion beam . The consequence of this is that the well implantation step has been divided into four steps and the costs for this step have thereby increased fourfold. However, the “quad implant” used makes it possible for the scattering to be produced only at the well edges which are the least critical.

[0006] The fabrication of DRAM semiconductor memory modules represents a very important application of well implantation. An explanation is given below, with

reference to Figures 2A and 2B, of a basic structure of known DRAM semiconductor memories, and the associated problem of well scattering.

[0007] Figure 2A shows a diagrammatic plan view of a small section of a DRAM 10. Situated on both sides of a line of symmetry S, which is indicated by a simple dashed line and runs horizontally in Figure 2A, are mutually adjoining p-type and n-type wells 12, 11, whose layout/circuit structures are mirror-symmetrical with respect to the axis of symmetry S. In Figure 2A, this is illustrated, for example, by the fact that mutually corresponding p-type wells 12 which are designated as a1, are arranged symmetrically with respect to the axis of symmetry S. The reason for this symmetry resides in the simple layout generation, or is historical. Consequently, the memory cells are produced by a mirroring process in a simple manner. The disadvantage of this mirroring process is illustrated by way of reference to a circuit structure at a side of the p-type well 12 which is designated by a1. If an a1 structure is exposed to a scattering radiation, brought about by an obliquely incident ion beam B, on one side of chip 10, the circuit a1 on the other side of the chip is not similarly exposed. The consequence of this fact is that the chip halves lying on opposite sides of the line of symmetry S are processed differently and, consequently, cannot be made identical.

[0008] To illustrate the above-outlined problem in further detail, a view from Figure 2A is depicted diagrammatically in Figure 2B. Two wells, namely an n-type well 11 and a p-type well 12, lie next to one another and are separated by a boundary G2. As already described with reference to Figure 1, during the implantation of n-type well 11, p-type well 12 is covered by a WP resist 3. Due to the scattering radiation at the edge of the WP resist layer, in the manner outlined above, the active components are

doped undesirably and influenced in a harmful manner in an edge region 13 of n-type well 11 which faces side a2 of p-type well. In the example illustrated with reference to Figures 2A and 2B, the undesirable doping applies to the active structures in n-type well 11 that lie below the line of symmetry S in the drawing, but, on account of the symmetry property, not to the corresponding active circuit structures in an n-type well 11 lying above the line of symmetry S.

[0009] In a similar fashion, during the implantation of p-type wells 12, n-type well 11 is covered by a WP resist, and during the implantation of the p-type well, well scattering adversely influences the corresponding active components in the p-type wells 12 on one side only of the line of symmetry S.

[0010] In light of the forgoing discussion, it is clear that a need exists to improve implantation processes, particularly as applied to DRAM memory fabrication.

SUMMARY

[0011] Consequently, it is an object of the invention to avoid the above-described problem in the fabrication of an integrated semiconductor circuit, in particular semiconductor memory circuit, and to enable such an integrated semiconductor circuit, in particular semiconductor memory circuit, in such a way that no harmful influencing of the parameter values of the active components occurs during the well implantation and, as a result, the reliability and service life of such an integrated semiconductor circuit is increased and the fabrication costs are reduced.

[0012] In an embodiment of the present invention, an integrated semiconductor circuit, in particular a semiconductor memory circuit, includes substrate contacts of the active components arranged to lie in direct proximity to an edge bounding the

mutually adjoining wells, and further includes other structures of the active components arranged to lie further away from said edge. Furthermore, according to an exemplary embodiment of the present invention, in an integrated semiconductor circuit comprising the aforementioned arrangement of substrate contacts and other structures, the circuit/layout structures are not configured mirror-symmetrically with respect to the center line of the semiconductor circuit chip.

[0013] In a DRAM semiconductor circuit according to another exemplary embodiment of the present invention, a p-doped well and an n-doped well are mutually adjoining, with the active components in the p-doped well having n-channel FETs and the active components in the n-doped well having p-channel FETs. Furthermore, the substrate contacts of the n-channel FETs in the p-doped well and the substrate contacts of the p-channel FETs in the n-doped well lie in direct proximity to a boundary between the two mutually adjoining wells.

[0014] In another embodiment of the present invention, a method for fabricating an integrated semiconductor circuit, in particular a semiconductor memory circuit, includes ion beam implantation with a specific irradiation angle oblique with respect to the crystal planes of the substrate. Further included is the use of ion beam implantation to implant mutually adjoining wells of a respective first and second conduction type in a substrate, as well as formation of active components and respective substrate contacts in the wells. In a preferred embodiment, the substrate contacts of the active components are formed in direct proximity to an edge between the mutually adjoining wells, while the other structures of the active components in the mutually adjoining wells are formed further away from said edge.

[0015] The above and further advantageous features are explained in more detail with reference to the drawings in the description below of exemplary embodiments of an integrated semiconductor circuit, which relates by way of example to a DRAM memory circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figure 1 illustrates a diagrammatic cross through an integrated semiconductor circuit for elucidating the “well scattering” phenomenon.

[0017] Figures 2A and 2B illustrate a plan view of essential circuit blocks of a known DRAM memory chip.

[0018] Figure 3 illustrates a plan view of circuit blocks of a DRAM memory configured according to an exemplary embodiment of the present invention.

[0019] Figure 4 illustrates a plan view showing an enlarged view of a portion of the DRAM memory chip depicted in Figure 3, including a region where wells adjoin one another at a boundary G, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0020] The following list of symbols is used consistently throughout the text and drawings.

- | | |
|----|------------------------------------|
| 2 | Active transistor region |
| 3 | Photoresist |
| 10 | DRAM chip |
| 11 | n-type well |
| 12 | p-type well |
| 13 | Critical region of the n-type well |
| 15 | n-FETs |
| 16 | p-FETs |

17 Contacts with respect to the p-type well
 18 Contacts with respect to the n-type well
 G, G1, G2 Boundary between p-type and n-type well
 B Ion beam
 M Center line
 S Line of symmetry
 α Irradiation angle of the ion beam
 a1, a2 Side regions of the p-type wells 12 that are occupied by the same
 circuit structures

[0021] In an embodiment of the present invention, a circuit/layout arrangement is altered from that of the conventional DRAM design, in conjunction with a “design rule” change. In a preferred embodiment, substrate contacts or bulk terminals are positioned in direct proximity to the edges, which scatter the implanting ion beam. One consequence of this arrangement is that the scattering implantation can even be utilized in a positive manner. In an exemplary embodiment, the contact implantation of the bulk terminals is thereby improved.

[0022] Preferably, the circuit/layout mirroring process heretofore employed in DRAM design is replaced by a non-mirror layout to avoid problems associated with implantation of mirror-symmetric chips discussed above.

[0023] Figure 3 diagrammatically shows a plan view with blocks of a DRAM memory chip 10 according to an exemplary embodiment of the present invention. In comparison with Figure 2A, which shows a similar plan view of a section of a known DRAM memory chip, in the case of the DRAM chip 10 shown in Figure 3, the circuit structures are not formed symmetrically with respect to the horizontal center line M. The n-type wells 11 all lie on the same side of the p-type wells 12. Moreover, by way

of example referring to the p-type wells 12, the mutually corresponding sides a1, which designate the same circuit structures in the wells, all point in one direction, and the other mutually corresponding sides a2 of the same well point in the opposite direction. A similar arrangement applies to the n-type wells 11. During the implantation of n-type wells 11 by means of ion beam B, which is incident at a specific angle, no well scattering occurs since the n-type wells all lie on one side, that is to say, on the side of the p-type wells at which no scattering of the ion beam B takes place.

[0024] Figure 3 also illustrates regions 13 in n-type wells 11, which adjoin the well boundaries G, and to which now, according to the above-described arrangement, are no longer critical with regard to the active components.

[0025] In an exemplary embodiment of the present invention, during implantation of p-type wells 12, the irradiation angle of ion beam B is altered or the wafer is rotated through 180°, such that the ion beam B is no longer scattered at the edges of the photoresist (which then covers the n-type wells) opposite the p-type wells.

[0026] It has been explained above with reference to Figure 3, in comparison with Figures 2A and 2B, on the basis of a DRAM memory circuit configured according to an embodiment of the present invention, that the mirror symmetry of the circuit structure and layout with respect to the center line M is canceled. As already mentioned, not only is the harmful effect of the scattering implantation avoided by the layout and the circuit structures no longer being mirror-symmetrical, but scattering implantation that nevertheless occurs, is utilized in a positive fashion by placing the substrate or bulk contacts in direct proximity to the boundary G between the two

mutually adjoining wells 11 and 12. The scattering implantation improves the contact implantation of the substrate or bulk terminals. This is illustrated in Figure 4, which depicts an enlarged plan view of a region of p-type well 12 and n-type well 11, on opposite sides of boundary G. In an exemplary embodiment, the numerals 17 and 18 designate substrate contacts of n-FETs 15 lying in p-type well 12, and p-FETs lying in n-type well 11, respectively. In a further exemplary embodiment, the numerals 17 and 18 designate bulk contacts of n-FETs 15 lying in p-type well 12, and p-FETs lying in n-type well 11, respectively. In both of the above embodiments, the contacts 17 and 18 are positioned in direct proximity to the boundary G between the two wells 11 and 12. The other structures of the active components lie further away from edge G. Therefore, in a preferred embodiment of the present invention, a necessary design rule change is implemented, which recognizes whether an active circuit structure, for example an FET, is sufficiently far away from boundary line G. By contrast, the substrate or bulk contacts 17 and 18 are intended to lie near to the well edge G in order thereby to improve the contact implantation of the substrate or bulk contacts.

[0027] In the above exemplary embodiment, integrated semiconductor circuits have been described by way of example on the basis of a DRAM semiconductor circuit. However, the principle of the invention can also be applied to other integrated semiconductor circuits, for example, when the intention is to avoid the harmful effect of the scattering implantation during well implantation by means of an ion beam in two adjacent wells occupied by active components.

[0028] The foregoing disclosure of the preferred embodiments of the present invention has been presented for purposes of illustration and description. It is not

intended to be exhaustive or to limit the invention to the precise forms disclosed.

Many variations and modifications of the embodiments described herein will be apparent to one of ordinary skill in the art in light of the above disclosure. The scope of the invention is to be defined only by the claims appended hereto, and by their equivalents.

[0029] Further, in describing representative embodiments of the present invention, the specification may have presented the method and/or process of the present invention as a particular sequence of steps. However, to the extent that the method or process does not rely on the particular order of steps set forth herein, the method or process should not be limited to the particular sequence of steps described. As one of ordinary skill in the art would appreciate, other sequences of steps may be possible. Therefore, the particular order of the steps set forth in the specification should not be construed as limitations on the claims. In addition, the claims directed to the method and/or process of the present invention should not be limited to the performance of their steps in the order written, and one skilled in the art can readily appreciate that the sequences may be varied and still remain within the spirit and scope of the present invention.